Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS

Claims 1-13. (Cancelled)

Claim 14. (Currently Amended) A power semiconductor device with trench gates comprising:

a semiconductor substrate;

a source layer on one surface of the substrate and comprising a high concentration of a dopant of one polarity;

a drift region lightly doped with said one polarity;

a single drain region on the other surface of the substrate;

a well layer beneath the source layer doped with a dopant of opposite polarity;

a plurality of trenches penetrating the source layer and terminating in said drift region, said trenches substantially filled with conductive material;

a highly conductive layer on the surface of the source layer comprising a material reacted from a metal and the semiconductor substrate;

an insulating layer on the highly conductive layer and on the conductive material in the trenches;

vias formed in the insulating layer and extending to the highly conductive layer on the source layer;

conductive material filling the vias for contacting the highly conductive layer.

Claims 15-19. (Cancelled).

Claim 20. (Previously Presented) The power semiconductor device of claim 14 wherein the trenches are filled with polysilicon and the top surface of the

polysilicon is covered with a highly conductive material reacted from a metal and the semiconductor substrate.

Claim 21. (Previously Presented) The power semiconductor device of claim 14 wherein the highly conductive layer is a silicide.

Claim 22. (Cancelled).

Claim 23. (Previously Presented) The power semiconductor device of claim 20 or 21 wherein the silicide is reacted from platinum or titanium.

Claim 24. (Previously Presented) The power semiconductor device of claim 14 wherein the insulating material on the highly conductive layer is BPSG, PSG, silicon dioxide or silicon nitride.

Claim 25. (Previously Presented) The power semiconductor device of claim 14 wherein the trenches are lined with a trench wall insulating material and the insulating material on the highly conductive layer contacts the ends of the trench wall insulating layer lining the walls of the trenches.

Claim 26. (Previously Presented) The power semiconductor device of claim 14 wherein one or more vias terminated on the surface of the highly conductive layer for making electrical contact between the highly conductive source layer and the conductive material filling the via(s).